Lecture 9

Registers and Counters

Outline

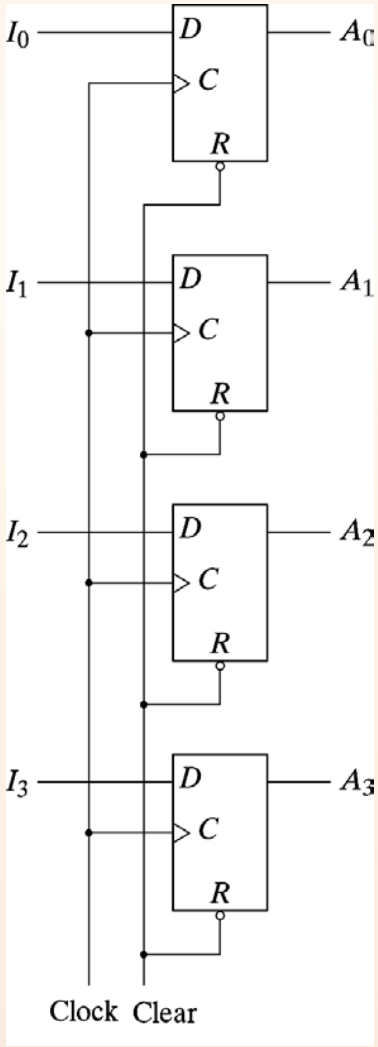
- Registers
- Shift Registers
- Ripple Counters
- Synchronous Counters
- Random-Access Memory

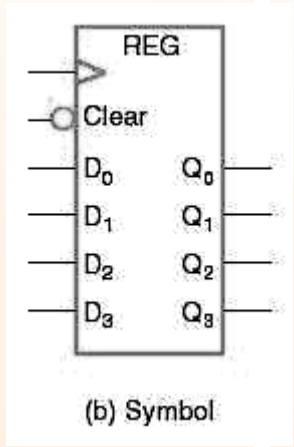
Registers and Counters

- Register:
  - A set of flip-flops, possibly with added combinational gates, that perform data-processing tasks
  - Store and manipulate information in a digital system
- Counter:
  - A register that goes through a predetermined sequence of states
  - A special type of register
  - Employed in circuits to sequence and control operations

The Simplest Register

- Consist of only flip-flops
- Triggered by common clock input
- The Clear input goes to the R (reset) input of all flip-flops
  - Clear = 0 " all flip-flops are reset **asynchronously**
- The Clear input is useful for cleaning the registers to all 0's prior to its clocked operation
  - Must maintain at logic 1 during normal operations

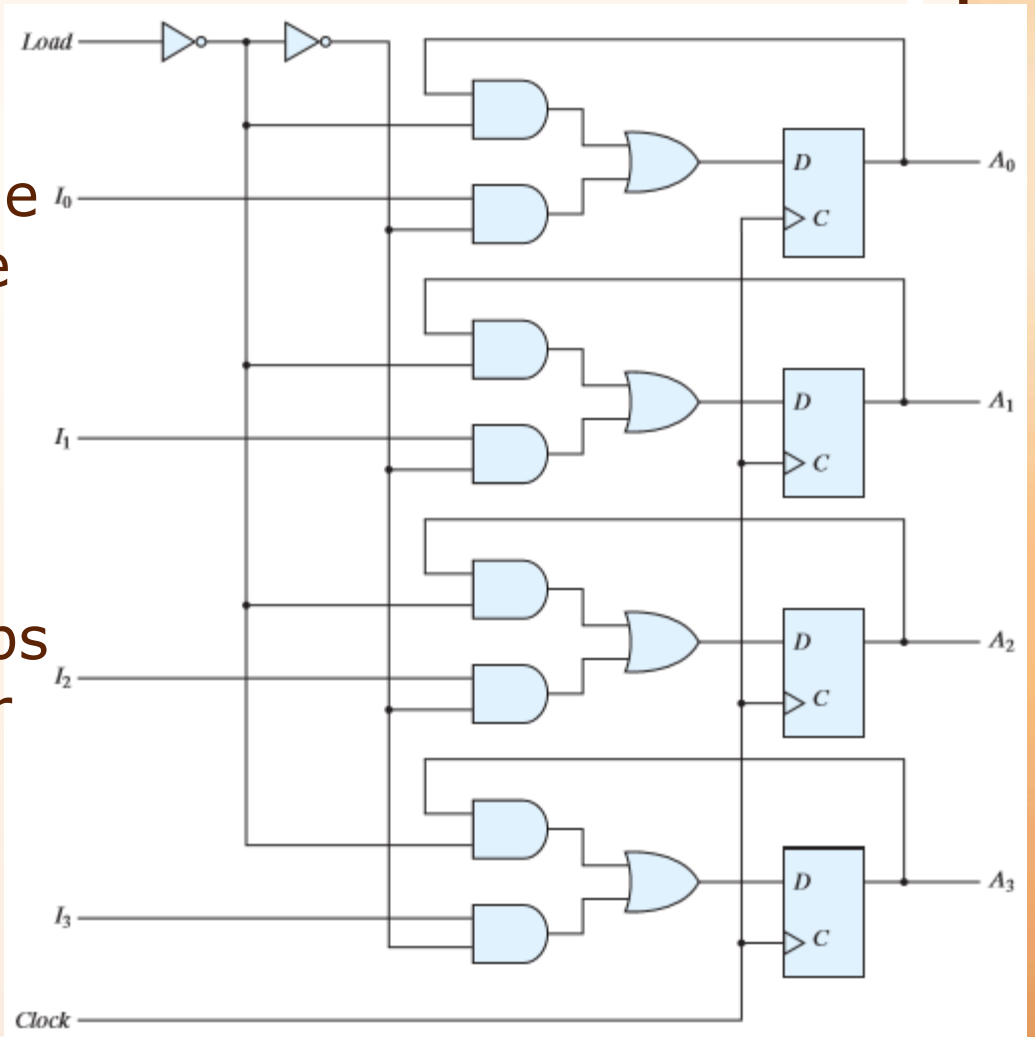




(b) Symbol

Register with Parallel Load

- When Load = 1, all the bits of data inputs are transferred into the registers
  - Parallel loaded
- When Load =0, the outputs of the flip-flops are connected to their respective inputs
  - Keep no change



The Simplest Shift Register

- Shift register: a register capable of shifting its binary information in one or both directions
- The simplest form: consist of only a chain of flip-flops in cascade

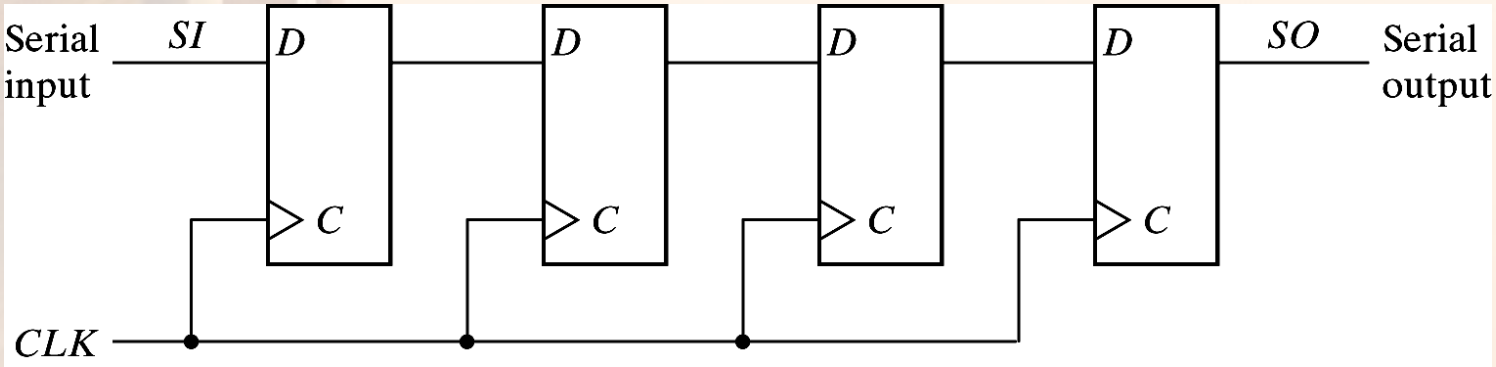
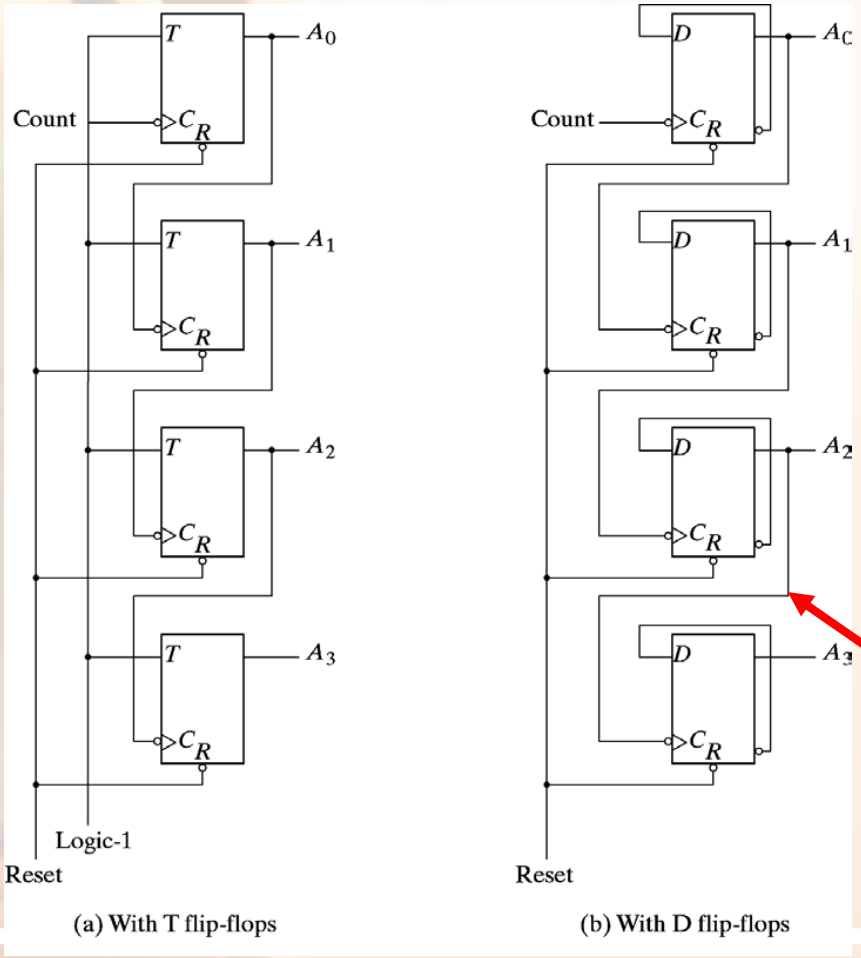


Fig. 6-3 4-Bit Shift Register

Binary Ripple Counter



Binary Count Sequence

A3	A2	A1	A0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

the output transition triggers the next flip-flop

BCD Ripple Counter

- The count will return to 0 after 9
- Q1: always complemented
- Q2: inverted when Q8 = 0 and Q1 =1→0
- Q4: inverted when Q2 = 1→0
- Q8: when Q1 = 1→0
- if (Q2 = Q4 = 1) Q8 is inverted
- else Q8 = 0

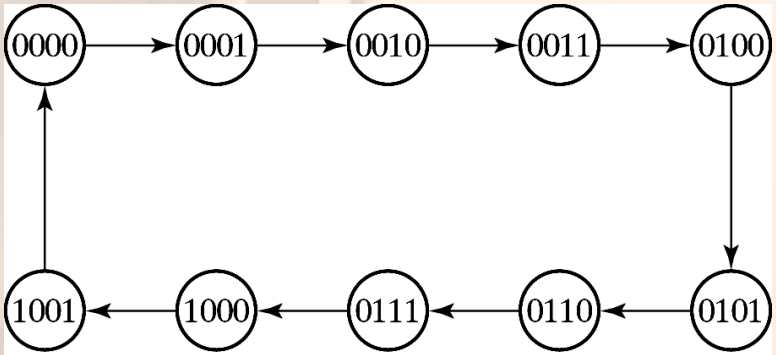
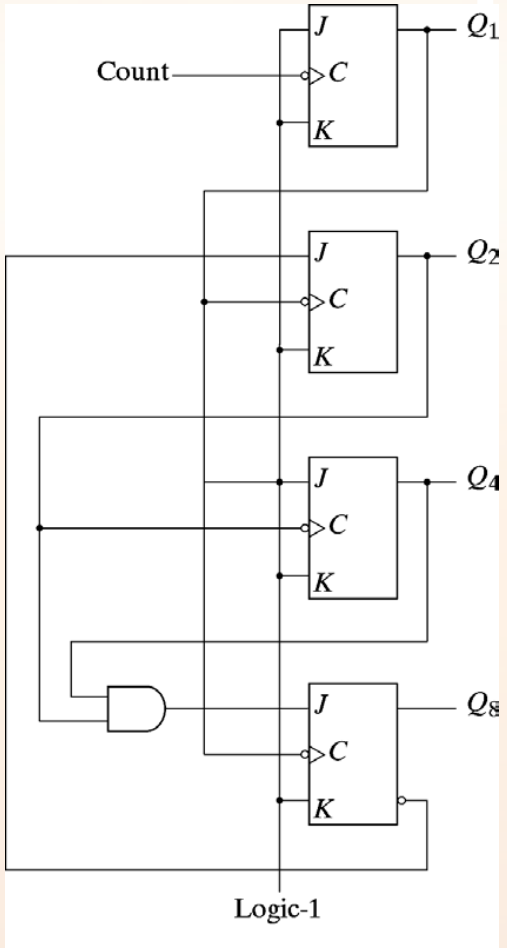


Fig. 6-9 State Diagram of a Decimal BCD-Counter



Ripple v.s. Synchronous

- Ripple counters:
  - Flip-flops are triggered by the outputs of another flip-flops
  - Triggering source may not the same for each flip-flop
  - The flip-flops are changed serially
- Synchronous counters:
  - Flip-flops are triggered by common clock pulses
  - Triggering sources are the same for all flip-flops
  - All operations are performed simultaneously

Design a BCD Counter

- Go through normal sequential circuit design procedure

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

$TQ_1 = 1$

$TQ_2 = Q_8'Q_1$

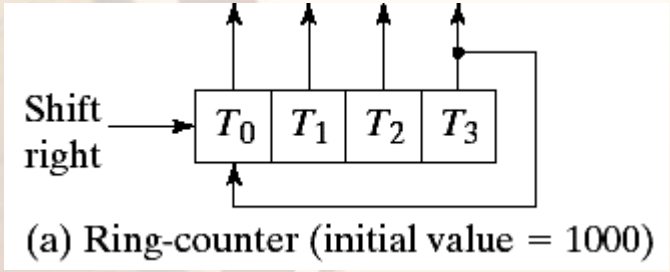
$TQ_4 = Q_2Q_1$

$TQ_8 = Q_8Q_1 + Q_4Q_2Q_1$

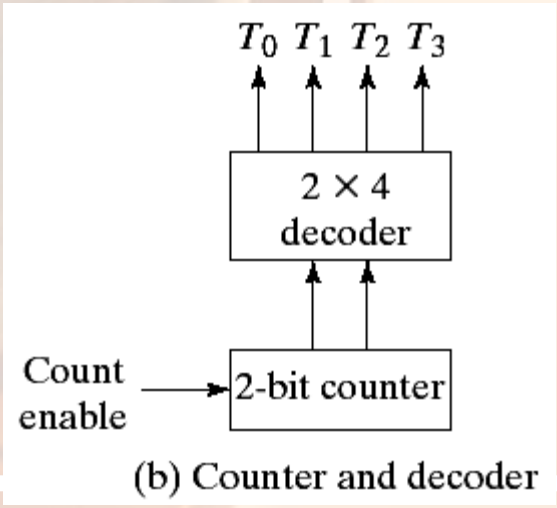
$y = Q_8Q_1$

Ring Counter

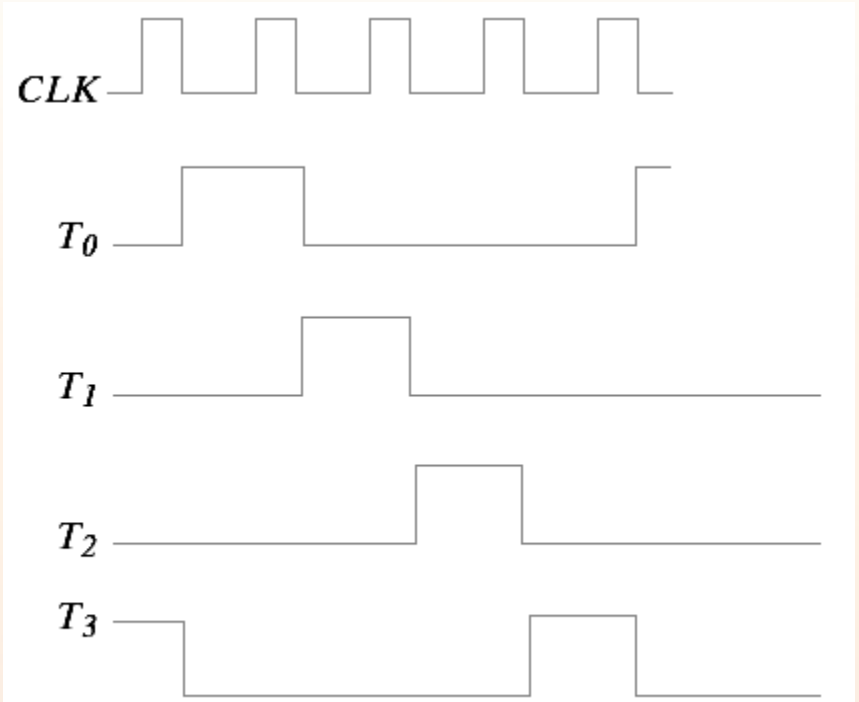
Ring counter: a circular shift register with only one flip-flop being set at any time



(a) Ring-counter (initial value = 1000)



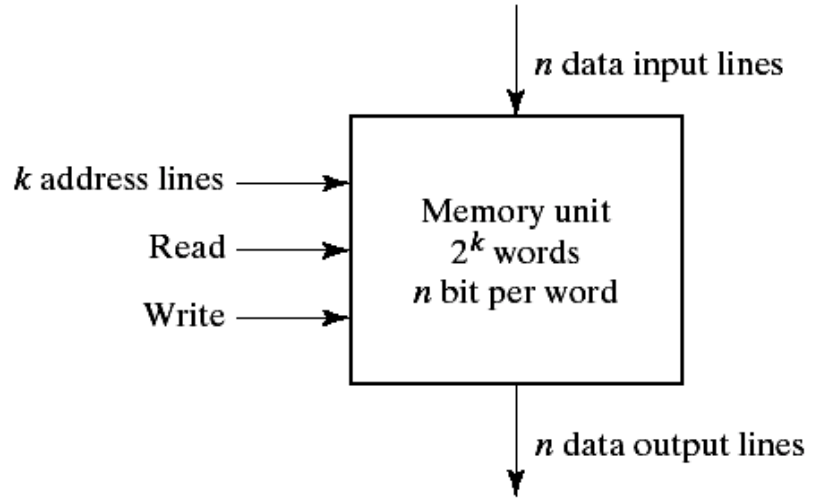
(b) Counter and decoder



(c) Sequence of four timing signals

Mass Memory Elements

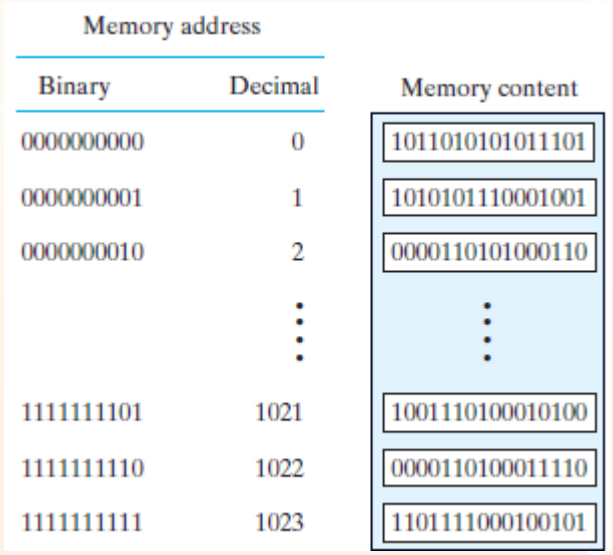
- Memory is a collection of binary cells together with associated circuits needed to transfer information to or from any desired location



- Two primary categories of memory:
  - Random access memory (RAM)
  - Read only memory (ROM)

Random Access Memory

- A **word is the basic unit that** moves in and out of memory
  - The length of a word is often multiples of a byte (=8 bits)
- Memory units are specified by its **number of words** and the **number of bits in** each word
  - Ex: 1024(words) x 16(bits)
  - Each word is assigned a particular **address, starting** from 0 up to 2^k -1 (k = number of address lines)



Memory address		Memory content
Binary	Decimal	
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

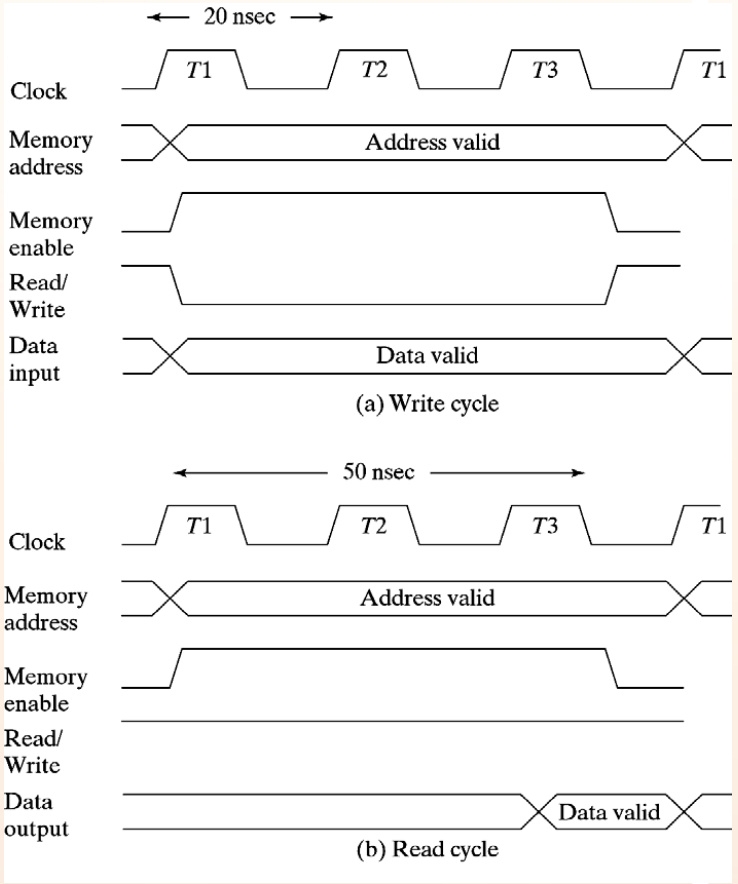
FIGURE 7.3:Contents of a 1024 * 16 memory

Write and Read Operations

- Write to RAM
  - Apply the binary address of the desired word to the **address lines**
  - Apply the data bits that must be stored in memory to the **data input lines**
  - Activate the **write control**
- Read from RAM
  - Apply the binary address of the desired word to the **address lines**
  - Activate the **read control**

Timing Waveforms

- CPU clock = 50 MHz
- cycle time = 20 ns
- Memory access time = 50 ns
- The time required to complete a read or write operation
- The control signals must stay active for at least 50 ns
- 3 CPU cycles are required



Types of Memories

- Access mode:
  - Random access: any locations can be accessed in any order
  - Sequential access: accessed only when the requested word has been reached (ex: hard disk)
- Operating mode:
  - Static RAM (SRAM)
  - Dynamic RAM (DRAM)
- Volatile mode:
  - Volatile memory: lose stored information when power is turned off (ex: RAM)
  - Non-volatile memory: retain its storage after removal of power (ex: flash, ROM, hard-disk, .)

SRAM vs. DRAM

- Static RAM:
  - Use internal latch to store the binary information
  - Stored information remains valid as long as power is on
  - Shorter read and write cycles
  - Larger cell area and power consumption

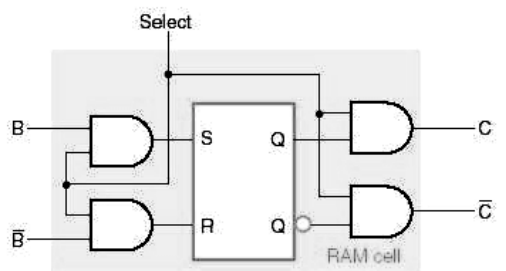
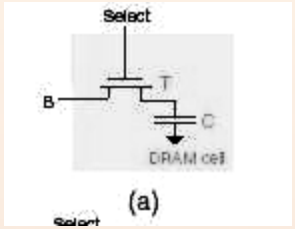
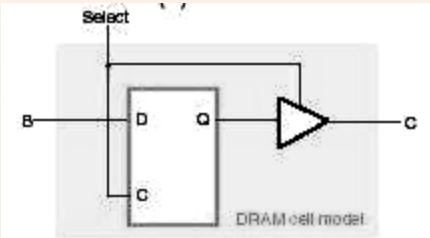


Fig. 6-5 Static RAM Cell

- Dynamic RAM:
  - Use a capacitor to store the binary information
  - Need periodically refreshing to hold the stored info.
  - Longer read and write cycles
  - Smaller cell area and power consumption



(a)



(h)

reading

- M. Morris Mano , Michael D. Ciletti “Digital Design With an Introduction to the Verilog HDL” FIFTH EDITION
  - Sections: 6.1 ,6.2(pages 255-259,266-275,280-281)
  - Sections: 7.1 ,7.2(pages 299-302)